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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,873	08/10/2004	Chethan Y.B. Kumar	TI-37555	4872
23494	7590	11/10/2005	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265				TSAI, CAROL S W
ART UNIT		PAPER NUMBER		
2857				

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

BK

Office Action Summary	Application No.	Applicant(s)
	10/710,873	KUMAR ET AL.
	Examiner	Art Unit
	Carol S. Tsai	2857

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 10 August 2004.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-16 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>4/12/2005</u>	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-16 are rejected under 35 U.S.C. 102(a) as being anticipated by U. S. Patent No. 6,606,575 to Miller.

With respect to claims 1, 2, 9, and 10, Miller discloses a machine readable medium carrying one or more sequences of instructions (see col. 4, lines 60-64) for causing a digital processing system (host computer 30 shown on Fig. 5) to control a test equipment to accurately place the edges of a signal used to test a device under test (DUT), performing the actions of: determining an expected time of occurrence of each edge of said signal (see Abstract, lines 4-6 and col. 8, lines 3-6 and lines 20-22); instructing said test equipment to generate a plurality of cycles of said signal in relation to said tester cycle time (see Abstract, lines 4-6 and col. 8, lines 3-6, lines 20-22, and lines 38-56); receiving data indicating a plurality of time points at which the edges of said signal have occurred in said plurality of cycles (see col. 5, lines 14-39); computing an error based on said plurality of time points and said expected time (see col. 8, lines 6-19 and lines 24-33); and adjusting a timing of the edges of said signal based on said error (see Abstract, lines 6-8 and col. 8, lines 33-37).

Miller does not disclose expressly execution of said one or more sequences of instructions by one or more processors contained in said digital processing system causing said one or more processors to perform the actions.

It is, however, considered inherent that Miller's host computer includes execution of said one or more sequences of instructions by one or more processors contained in said digital processing system causing said one or more processors to perform the actions (see col. 5, lines 14-18), because a host computer including a program, stored at memory and executed at processor, is known to be necessary element in order to receive, store, analyze, or display data acquired from data acquisition system.

As to claims 3 and 11, Miller also discloses said plurality of time points comprising at least ten time points (see Figs. 6-8).

As to claims 4, 5, 12, and 13, Miller also discloses sending a command to configure a device under test (DUT) interface board to loop back said signal to said test equipment (see col. 9, lines 29-44).

As to claims 6 and 14, Miller also discloses determining a mean value of said plurality of time points; and setting said error to equal a difference of said mean value and said expected time (see col. 9, lines 45-53).

As to claims 7 and 15, Miller also discloses the edges of a clock signal being placed accurately by using said clock signal as said signal, and the edges of a data signal being placed accurately by using said data signal as said signal such that said data signal can be sampled accurately using said clock signal in said DUT (see col. 3, lines 2-35; col. 4, lines 15-20; and col. 7, lines 39-44).

As to claims 8, and 16, Miller also discloses sending to said test equipment a threshold voltage level indicating a voltage level, said threshold voltage level at which said signal is deemed to have transitioned from one logic test equipment compares said a voltage level of said threshold voltage level to signal a plurality of times in each level to another, wherein said tester cycle and provides a comparison result, wherein said data comprises said comparison result and a time of comparison (see col. 8, lines 38-56).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gutnik et al. disclose a digital circuit includes a plurality of arbiters, each arbiter having first and second input ports and an output port at which is provided an arbiter output signal.

Nelson discloses an output-relative signal receiver to test an integrated circuit that provides an output-relative data signal.

Schaber et al. disclose a driver circuit for use on an integrated circuit tester.

Maassen et al. disclose method and apparatus for calibrating timing accuracy during testing of integrated circuits.

Frisch et al. disclose an integrated circuit tester channel including an integrated circuit for adding a programmably controlled amount of jitter to a digital test signal to produce a DUT input signal having a precisely controlled jitter pattern.

Chenoweth et al. disclose a system for testing an integrated circuit device under test

(DUT) communicating through synchronous digital signals and through a high speed serialization/de-serialization (serdes) bus including a serdes interface circuit for communicating with the DUT via the serdes bus and an integrated circuit (IC) tester for communicating with the DUT and with the serdes interface circuit via digital signals.

Contact Information

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carol S. W. Tsai whose telephone number is (571) 272-2224. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 886-217-9197 (toll-free).



Carol S. W. Tsai
Primary Examiner
Art Unit 2857

cswt
November 3, 2005